ENPH 455/555 Thesis

Schlieren system for flow visualization with integrated circuit for high frequency LED pulsing

by

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Abstract

Schlieren system is designed for flow visualization of detonation waves through a narrow channel. The design process includes determining the setup that best fits within the spatial constraints of the lab, designing a PCB for high-frequency LED pulsing, and determining the setup that produces the best quality Schlieren image. The setup of the schlieren system involved centering all optical components, calculating the appropriate angles at which to tilt the parabolic mirrors, light source, and camera to minimize optical aberrations, and adding a flat mirror. The flat mirror was placed at a 45-degree angle between the first and second parabolic mirrors. The flat mirror redirected the light so it could pass through the flow visualization section of the detonation channel.

High-frequency LED pulsing requires a PCB that maintains signal integrity at high edge rates. Two circuits were designed to increase the current of the signal received by the LED driver. Both circuits used a high slew rate op-amp along with appropriate decoupling capacitors and feedback resistors. One circuit implemented the Sallen-Key filter topology, while the other did not. These designs are compared to determine which provides the best performance. The PCB layout consists of a four-layer design. The via placement, trace spacing and length, component placement, thermal management, impedance control, and grounding of the design are discussed.

Acknowledgments

This project could not have been completed without the support of Dr. Jackson Crane, my thesis advisor, and members of the Crane Energy Group. Dr. Crane and his team has provided me with endless support and encourage me on this project.

Chapter 1

Introduction

Detonation occurs during supersonic combustion when the leading shock wave compresses the gas to the point of self-ignition. [1] The interaction between the leading shock and the induced secondary shock waves causes spatial and temporal fluctuations. These fluctuations are non-linearly coupled to the reaction front behind the shock which sustains the detonation flame. [2] Due to the nature of the detonation process being considered constant in volume, the energy efficiency is much greater than that of subsonic combustion. However, there are inherent instabilities due to complex interactions within the leading shock, the induced shock, and the reaction front. Research is being conducted to mitigate these instabilities, but conducting the research requires a method to visualize the detonation structure.

Schlieren flow visualization process for detonation is a common approach to image the cellular structure of detonation waves. Schlieren works by capturing changes in the refractive index as light passes through an interface, in this case, the interface between the air and the flow. [3] The density gradients in the flow, due to the changes in temperature and pressure, cause varying refractive indexes. These gradients are picked up by a high-speed camera, revealing the structure of the flow.

The purpose of this project is to design a schlieren system for the Crane Energy Group. The system must be designed to fit within the spatial constraints of the lab and be able to produce a clear image of the detonation structure for analysis. Typically, researchers use a constant light source for schlieren imaging, however, this project will utilize high frequency LED pulsing in order to decrease image blur between shutters, increase the effective shutter speed, and ultimately produce a higher quality image. High frequency LED pulsing requires the use of a LED pulse driver and a signal generator. The models of choice are the Picolas LDP-V-03-100 and the NI-6356 USB DAQ respectively. Interfacing these devices requires designing and integrating a PCB to increase the current from the DAQ to drive the Picolas. Successful completion of the project will entail developing a fully functional schlieren system with a point light source, the ability to produce high quality images, and a functioning high-speed PCB.

Chapter 2

Results and Analysis

2.1 Schlieren

2.1.1 Point Light Source

The laser diode setup consists of three key components for proper implementation. These components are the diode, collimating lenses, and iris. [3] The diode chosen is Thorlabs LED635L. This diode can handle the system requirements and operates normally at 2.3V and 350milliamps of current. The LED is not a point source thus collimating lenses and an iris are required to have the light emit as a point source. The collimating lenses are two aspheric condenser lenses. The flat side of the first lens faces the LED and the convex side of both the lenses face each other as shown in figure. The LED and iris must be aligned at the focal length of the lenses. [4] The lenses themselves can be separated by any length due to collimation, however it was found that best results were shown when the distance was the focal length. Likely due to imperfect collimation as the LED is not a perfect point source. The iris is placed after the second lens and should be adjusted to the smallest size to best simulate a point source.

The alignment of the laser diode is crucial for proper focusing. A cage system was used to properly align each optical component in horizontal and vertical plane. Careful measurements were taken using calipers to set each component at the appropriate location. A laser target was used to determine if the LED is at proper focus. The LED is properly focused when the beam reaches the iris at a point and then begins to expand after it passes through. [4]

2.1.2 Schlieren Apparatus

The apparatus includes two parabolic mirrors with kinematic mounts, a mounted flat mirror, a knife edge, a camera, and a point light source. The system utilized is a z-type schlieren in an L configuration to account for the shape and size of the room as shown in Figure. 2.1. The light source faces the first parabolic mirror at an angle of 7.2 degrees from the center line and they are separated by a distance equal to the focal length of the parabolic mirror, 100 inches. The mirror is tilted at an angle of 3.6 degrees towards the light source. These angles were calculated to minimize astigmatism effects, Eq. 2.1. [3] The first parabolic mirror faces a flat turning mirror, which placed in front of the detonation channels visualization section, and is angled at 45 degrees towards the second parabolic mirror. The second parabolic mirror and camera are angled at equal but opposite directions from the first mirror and light source respectively. The equal and opposite angles eliminates coma effects. The knife edge is placed in front of the camera for density gradients to be visualized. The knife edge will be eventually be replaced by a circular cut to allow for visualization of all density gradients. [3] The amount of cutoff will be varied to depending on the desired image.

$$\Delta f = \frac{f \sin^2(\theta)}{\cos(\theta)} \tag{2.1}$$

Slight adjustments of the turning mirror were required to produce the desired image. The mirror was susceptible to bending when placed in the mount. This bending caused beam to deflect non uniformly resulting in undesirable images. A new thicker mirror was purchased and the issue was solved.

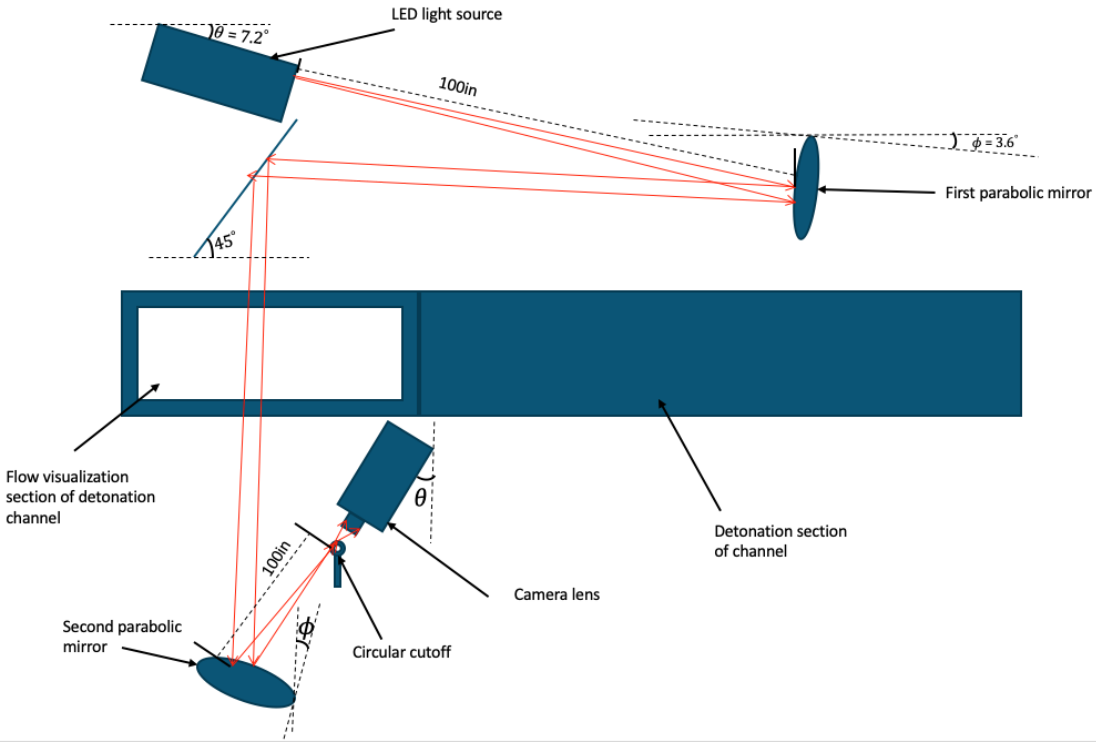


Figure 2.1: Diagram illustrating the schlieren optical setup.

2.1.3 Schlieren Final Design and Results

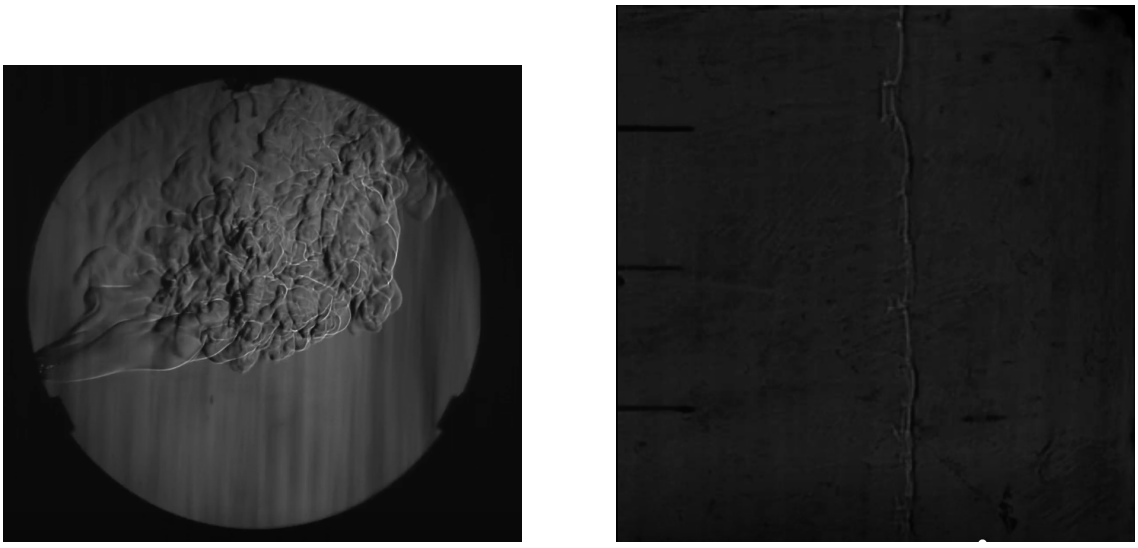
The first images generated were shadowgraph as it was challenging to perfectly align the system for Schlieren. The shadowgraph images clearly show the propagating wavefront however the details are not as exaggerated as schlieren.

Schlieren was eventually achieved after finely adjusting the heights and angles of the optical components. Aligning the mirrors was a significant challenge especially given the setup of the lab. The placement of the turning mirror needed to be exactly correct so the light would approach the parabolic mirrors at the correct placement. The process for aligning the optics involved first setting the appropriate angle between the light source and the first parabolic mirror. Then creating a center line from the parabolic mirror to the turning mirror and placing the turning mirror in the path of the light at 45 degrees. Then matching the other parabolic mirror to the opposite angle of the first parabolic mirror to the turning mirror. After the initial alignment fine adjustments were made until the light focused to a clear point at the focal length of the second parabolic mirror. After fine adjustments of the angles the best results were achieved when the mirror was tilted at an angle of 3.15 degrees towards the light source and the source faced the parabolic mirror at an angle of 6.3 degrees from the centerline. The angles slightly deviate from the calculated angles likely due to experimental error. The measuring device has an error of 0.1 degrees, and when factoring in an additional error 0.5 degrees due to the manual alignment of the device and centerline strings, the total error is 0.51 degrees, Eq. 2.2. The measurement is therefore within error of the calculated value. The effect of adding a turning mirror may have also contributed to the difference in the calculated and experimental angles as the calculation does not account for the turning mirror.

$$\sigma = \sqrt{\sigma_x^2 + \sigma_y^2} \tag{2.2}$$

Schlieren and Shadowgraph images are shown in Fig. 2.2. The Schlieren image used a vertical knife edge cutoff of 50% [3], therefore cutting of horizontal density

gradients. Schlieren has not yet been used for a detonation test so the image shown is a flame from a blow torch. The Shadowgraph image is from a detonation test. The wavefront is clearly visible however the details of the wavefront are not as defined as that from the Schlieren image.



(a) (b)

Figure 2.2: Schlieren and Shadowgraph images. Fig. a) is a Schlieren image of a blow torch flame at 50% cutoff. Fig. b) is a Shadowgraph image of a detonation wave

2.2 PCB design process

2.2.1 Design Requirements

The requirements of the design are that the signal rise time at the output must be one nanosecond or faster, the output signal must not drop below 4.7 Volts or above 5.3 Volts, and the PCB must connect to the signal generator, Picolas, and a power supply.

PCBs with rise times of one nanosecond or less require careful consideration when designing. Proper grounding techniques, trace impedance, component placement, and trace separation will all need to be considered to retain signal integrity at high speed. The rise time of the design will be evaluated based on how close the actual rise time is to the calculated one.

The Picolas supports trigger voltages in the range of 4.7V to 5.3V. Noise can cause the voltage to oscillate outside of this range and damage the device. [5] Therefore, high signal integrity is paramount for a successful design. However, at high edge rates there is a greater risk of crosstalk noise between signals. [6] Careful consideration of component and trace spacing is required to minimize this noise. The design will be evaluated on how the output voltage compares to the input and how close the actual settling time is to the calculated one.

To integrate the PCB with the required devices, a coaxial cable will run from the output of the signal generator to the input of the PCB. The output of the PCB will be connected to the input of the pulse driver via another coaxial cable. The power to the PCB will be connected with banana clips to a power supply. A Faraday cage will surround the PCB to prevent external noise from affecting the signal. The design will be evaluated on how well the PCB is shielded and how easily the coaxial cables and power cables are connected.

2.2.2 Circuit Design Process

The initial circuit design utilized a NPN and PNP transitor in the configuration shown in Figure. 2.3. The design used the two transistors to maintain an output voltage within the desired range. The base-emitter voltage for both transistors is around

0.7V. The NPN transistor is in the active region when the base voltage is equal to the emitter voltage plus the base-emitter voltage as shown in Eq. 2.3. Allowing current to flow from the collector to the emitter.

$$V_b = V_e + V_{be} \tag{2.3}$$

For the PNP transistor, the base-emitter voltage is negative. Thus, for the transistor to be in the active region, the base voltage must be equal to the emitter voltage minus the base-emitter voltage, allowing current to flow from the emitter to the collector. [7] Therefore, to maintain a signal within the desired voltage range an NPN and PNP transistor must be connected. The current at the output is amplified as shown in Eq. 2.4. When the transistor is in the active region the collector current is equal to the base current multiplied by the current gain. The emitter current is amplified by increasing the base current.

$$I_c = \beta \cdot I_b \tag{2.4}$$

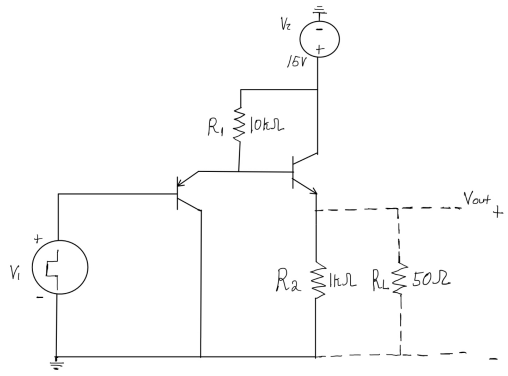


Figure 2.3: The initial design of the circuit. R1 was varied from 4.7kohms to 10kohms to determine the best response.

The design was tested using a breadboard, Fig. 2.4. Unfortunately the noise was greater than desired, and the rise time significantly exceeded the requirement of one nanosecond or less. Finding the appropriate transistors and determining the best configuration posed a significant challenge. To solve this problem the transistors were replaced with a high speed current feedback amplifier in both final circuit designs.

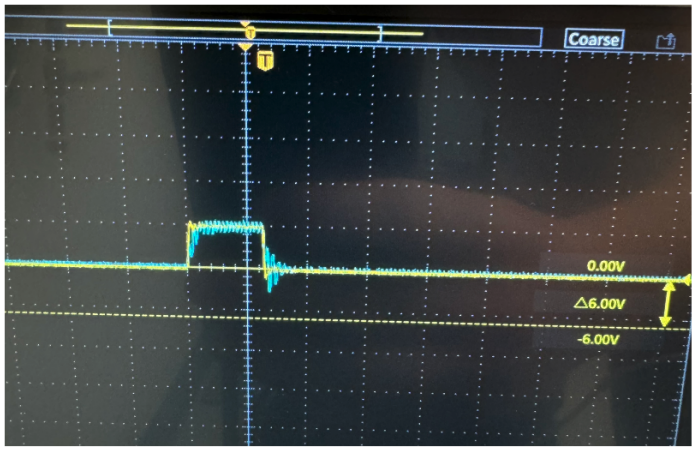


Figure 2.4: Oscilloscope reading for the initial circuit design. R1 was set to 10kohm. The transistors used were the 2N2222 NPN transistor and the 2N3904 PNP transistor

The final two circuit designs consisted of similar components. The first design implemented the THS3001IDGR current feedback amplifier in a non inverting configuration, Fig. 2.5(a). The second designed implemented the same amplifier and configuration, however a sallen key filter topology was included, Fig. 2.5(b). The slew rate of the chosen amplifier is 6500V/µs corresponding to a rise time of 0.615ns, Eq. 2.5.

$$t_r = \frac{4.5 - 0.5}{\text{Slew Rate}} \tag{2.5}$$

The output current of the amplifier is 100 milliamperes, which is needed to drive the Picolas. A feedback resistor is required to maintain stability of the amplifier and it

is recommended to use a 1kohm feedback resistor. [8] To keep the voltage below the given threshold, a gain resistor of 49.9kohms was chosen, resulting in a gain of 1.02, Eq. 2.6.

$$V_o = \frac{R_g + R_f}{R_g} V_i \tag{2.6}$$

The recommended ceramic decoupling capacitors along with tantalum bulk capacitors are connected to the power pins on the chip in order to filter out high frequency noise from the power supply and stabilize the voltage. [8] Finally, a 49.9ohm terminating resistor is placed at the input. This impedance matches the characteristic impedance of the chosen SMC coaxial cable, Eq. 2.7. Impedance matching prevents signal loss due to reflection from occurring by keeping the refractive indexes the same at the interface. [9]

$$Z_{\text{in}} = Z_{\text{O}} \frac{Z_L + jZ_{\text{O}} \tan(\beta l)}{Z_{\text{O}} + jZ_L \tan(\beta l)} \tag{2.7}$$

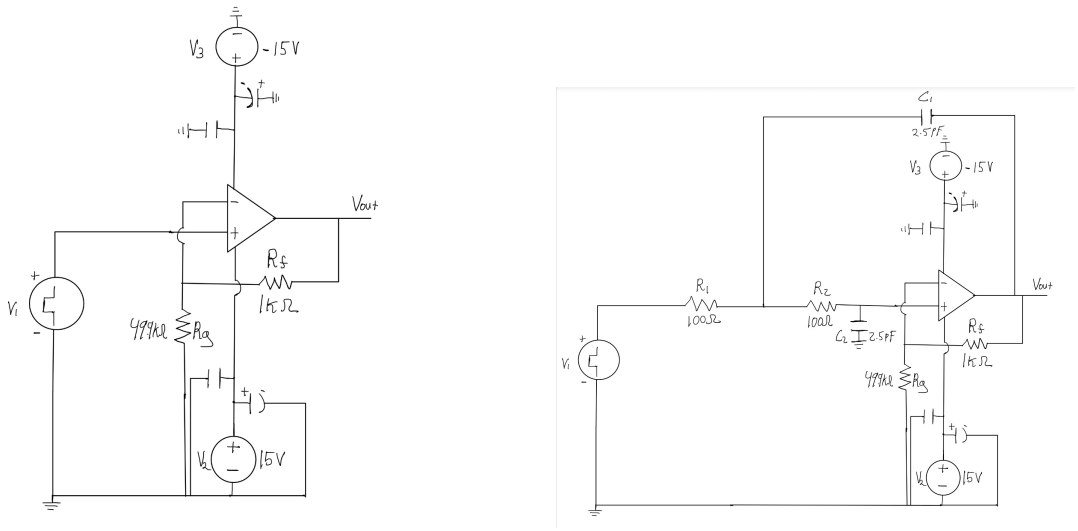
The sallen key-filter topology was implemented in an attempt to control the settling time, damping, and to filter high frequency noise. [10] To achieve a settling time of one nanosecond and ensure a damping ratio of one, a resistance of 100 ohms and a capacitance of 2.5 picofarads are used, Eq. 2.8. The capacitance and resistance values were calculated from the transfer function, Eq. 2.9.

$$t_s = \frac{4}{\omega_n} \tag{2.8}$$

$$\frac{V_o}{V_i} = \frac{\frac{1}{R^2C^2}}{S^2 + \frac{2}{RC}s + \frac{1}{R^2C^2}} \tag{2.9}$$

$$t_r \approx \frac{\pi}{\omega_n} \tag{2.10}$$

The rise time was calculated to be 0.785ns, Eq. 2.10, which is under the maximum acceptable rise time. The circuit is designed as a low pass filter with a cutoff frequency of 637 megahertz. The bode plot shown in Fig. 2.6 illustrates the frequency response for the filter.



(a) (b)

Figure 2.5: Circuit diagrams of the two final designs. Fig. a) is the circuit for the Non Sallen-key filter design and Fig. b) is the circuit diagram with the Sallen-key filter

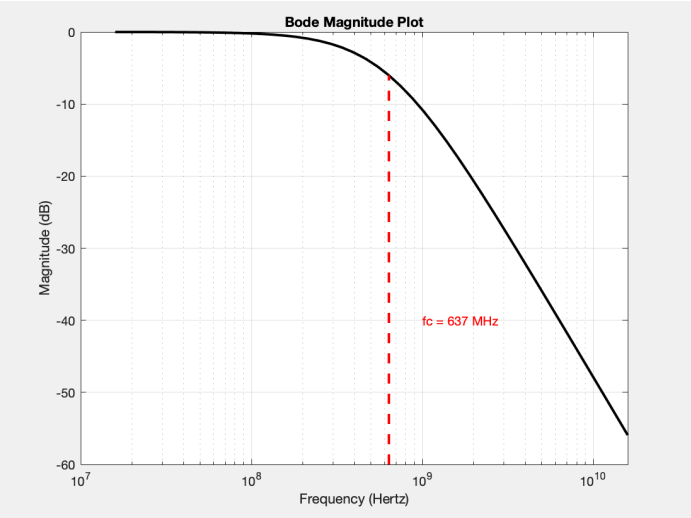
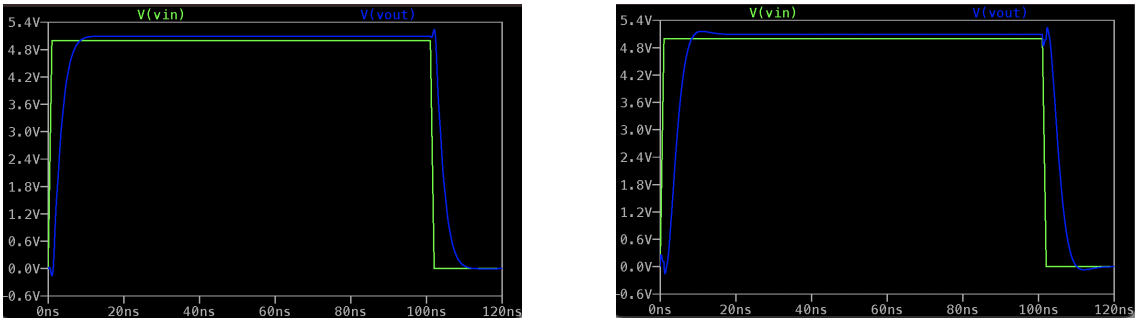


Figure 2.6: The bode plot shows the Db roll off with respect to the frequency. The cutoff frequency for the circuit is 637MHz.

Simulations for the final circuit designs were conducted using LTSpice, Fig. 2.7. A model of the THS3001IDGR was not available in the simulation software, so the AD811 current feedback amplifier was chosen. The characteristics of the AD811 are very similar to that of the THS3001IDGR, however, the slew rate of the AD811 is 2500V/µs. The simulations matched the expected results. No significant difference was evident in the simulation with the two designs. This was to be expected as no noise was introduced into the simulation. However, the simulation of the circuit without the Sallen-key topology provided slightly less overshoot. Indicating that it would be a better choice to not include the Sallen-key topology unless noise filtering was needed.



(a) (b)

Figure 2.7: Simulations of the two final designs. Fig. a) is the simulation for the Non Sallen-key filter design and Fig. b) has the Sallen-key topology

The design illustrated in Fig. 2.5(a) was tested using a breadboard. The THS3001IDNR was soldered onto a 8-pin SMD to DIP adapter for breadboard compatibility. The output of the circuit was connected to the Picolas and to the oscilloscope. The output of the DAC was connected to both the input of the circuit and the oscilloscope. The oscilloscope reading is shown in Fig. 2.8.

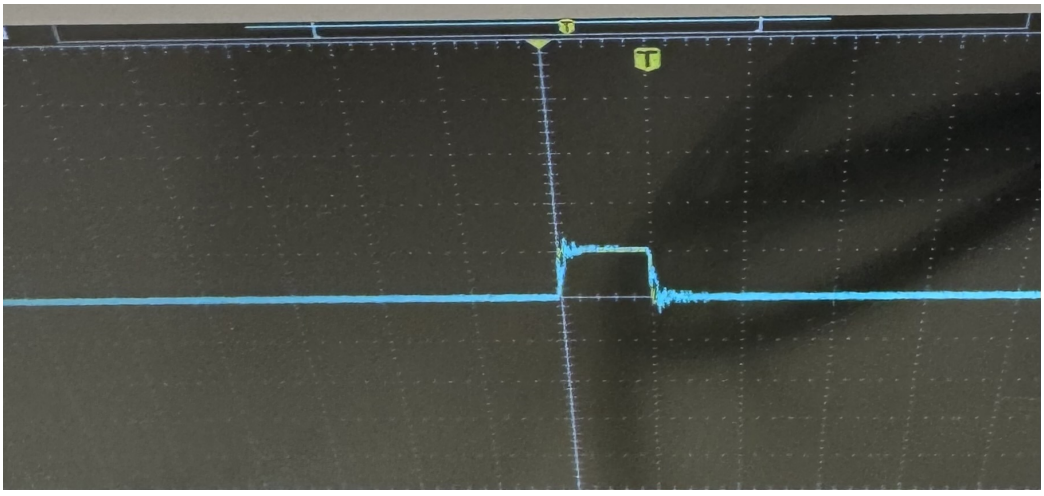


Figure 2.8: Oscilloscope reading of the first final design without the sallen key filter. Blue line is the circuit output and the yellow line underneath is the input.

This design performed much better than the initial design. The noise of the signal was reduced significantly and the rise time was decreased to 40 nanoseconds. Although the circuit can operate at faster edge rates it is limited by the breadboard and jumper cables. Breadboards contain stray capacitance between pins, which affects signal integrity. Additionally, jumper wires are not well shielded, leading to signal loss during rapid changes in the electric field. [11] To achieve the required signal integrity and rise time, a PCB must be designed.

2.2.3 PCB Layout

The layout of the PCB is very critical for high speed designs to maintain signal integrity. Many factors affect signal integrity, but the most significant factors are proper grounding, trace spacing, impedance matching, and component placement.

For proper grounding the return current must be considered. The return current follows the shortest path through the reference ground, which is the path of least impedance. In order to provide the best reference ground plane, the bottom plane should be almost completely grounded. [12] Therefore, the amount of traces in the back must be minimized. Currently, there are three short traces on the bottom of the board. These traces are used only to pass traces on the top plane. The bottom plane traces are aligned perpendicular to the top plane traces to prevent capacitive coupling. Improper grounding may lead to ground loops which can induce a current. To prevent this, the ground from the power supply and the signal ground are connected on the ground plane. The connections are well distributed across the plane and any current induced would be negligible. However, whenever possible the grounds should be connected at one point to eliminate the possibility of ground loops.

Crosstalk is amplified at high speeds as the strength of parasitic capacitance between traces is increased, therefore trace spacing is important. In order to minimize this effect the traces are separated by at least three times their width. For traces that are too close together, via's are used to prevent coupling by providing a strong return path and separating the traces. The spacing between via's is calculated using Eq. 2.11 to prevent resonance at the emitted frequency. [13] Vias are also placed near signal transitions to provide a return path for the current. Traces positioned too close to the ground plane may also lead to capacitive coupling, impacting circuit performance. To mitigate this, the spacing between traces and the ground plane should be at least three times the trace width. This consideration is particularly crucial in controlled impedance designs, where parasitic capacitance can significantly influence the trace's overall impedance. [14].

$$S = \frac{c}{8f\sqrt{\epsilon_r}} \tag{2.11}$$

Impedance control is important for PCB design to prevent signal loss and reflection. To properly control trace impedance, the layout consists of four layers: signal/ground, ground, power, and signal/ground. The impedance of the traces is dependent on the dielectric constant of the substrate, the width of the trace, and the spacing between the trace and the substrate below it, Eq. 2.12. Therefore, to control the impedance without requiring the trace width to be very large, the ground plane underneath the trace must be as close to the trace as possible. The ground plane is much closer to the traces in a four layer design compared to a two layer design.

$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \cdot \ln\left(\frac{5.98h}{0.8W}\right) \tag{2.12}$$

Component placement also plays a role in maintaining signal integrity. Components are placed to minimize the amount of traces on the bottom plane and to prevent traces from being too close to each other. Decoupling capacitors are placed as close as possible to the chip for better performance as trace resistance and inductance are decreased. [15]

2.2.4 First Tested PCB Design

The fist PCB design that was tested was reached after multiple iterations of the original design. The original design was a two layer board but it was determined to be insufficient due to the lack of impedance control. The board used for testing and is shown in Fig. 2.9.

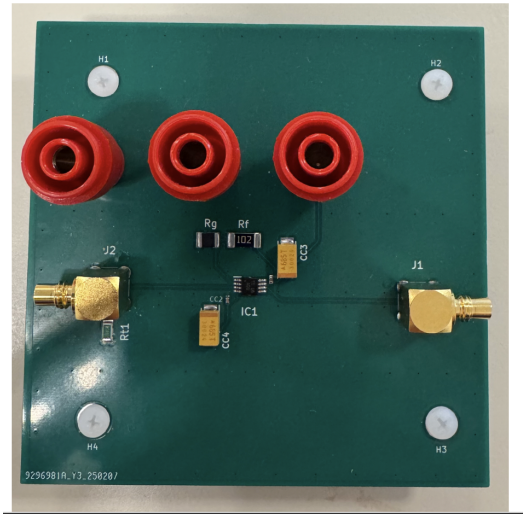


Figure 2.9: Printed and soldered PCB used in the first test

The board was able to achieve the desired rise time, but the overshoot and settling time was greater then expected, Fig. 2.10. The high overshoot is likely due to either signal refections, high input capacitance at the negative terminal, or external noise.

The Sallen-key filter design has not yet been tested and may help reduce the initial overshoot. The Faraday yet been implemented, but it should eliminate external noise from effecting the system. The amplitude of the pulse was half of what was originally expected. This was determined to be due to the terminating resistor on the PCB and the load resistance of the picolas being in series. The resistance doubles which results in the voltage being halved. To reach the desired voltage of 5V the 49.9kohm gain resistor is replaced with a 1kohm gain resistor resulting in a gain factor of two, Eq. 2.6.

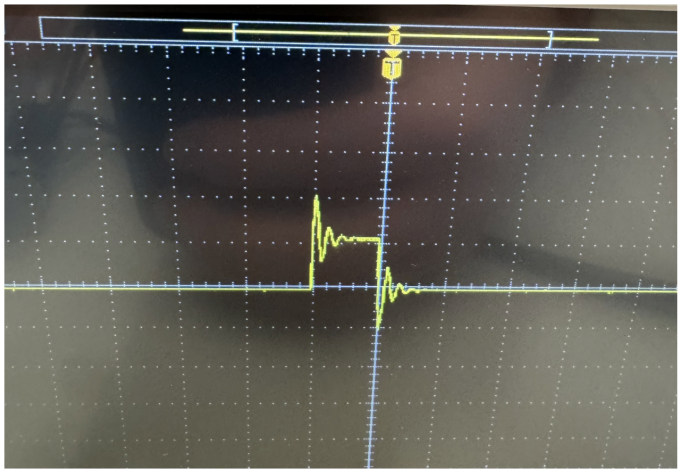


Figure 2.10: Oscilloscope reading of the first tested PCB design. Pulse width is 400 nanoseconds and amplitude scale is set to 2.5V/division

2.2.5 Final PCB Design

Slight modifications to the previous design were completed for better performance. The adjustments included: Adding a complete array of stitching vias for better connection between the ground planes, adding more stitching vias near transitions to provide a shorter path for return current, a shorter feedback line and more of the

ground plane removed from below it to limit the capacitance at the negative terminal, and wider spacing between the microstrips and the ground plane. The complete Kicad design is shown in Fig. 2.11.

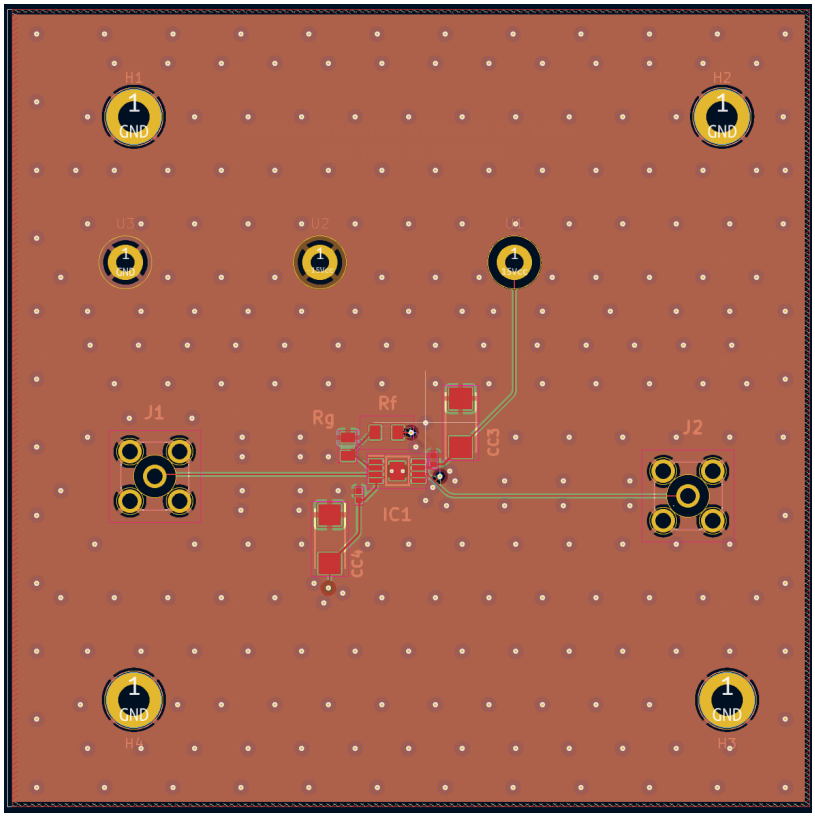


Figure 2.11: Kicad model of the modified final PCB design.

The modified design was tested and generated the expected output while connected to the picolas. The rise time, settling time, and amplitude where all within the required range, Fig. 2.12. The sallen-key filter topology was not tested because the designed function correctly without the filter. Adding the filter would have likely only increased the signals rise time.

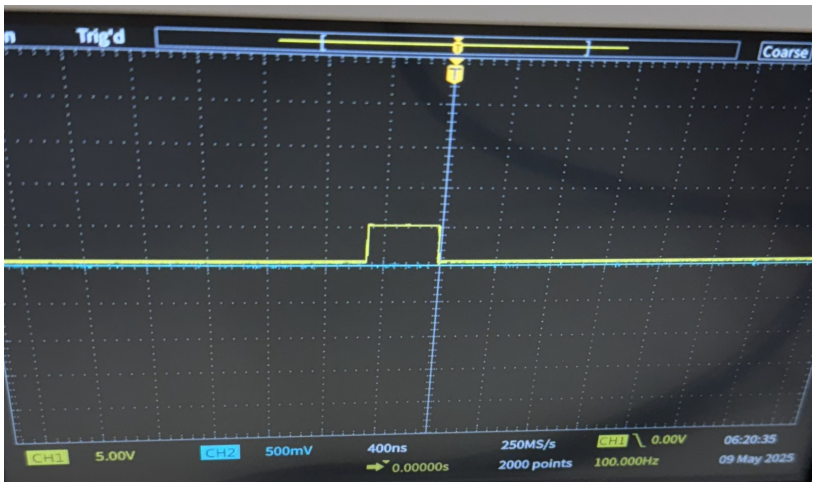


Figure 2.12: Oscilloscope reading of the final PCB design. 400 nanosecond pulse width and amplitude set to 5V/div

2.2.6 Pulsing the light source

The PCB was connected to the Picolas using two 50 ohm impedance coaxial cables. One cable running from the DAQ to the PCB and the other running from the PCB to the Picolas. Both the Picolas and the PCB were powered with the same 15V power supply. The LED was soldered as close to the Picolas as possible to minimize the signal rise time measured from the scope pin on the Picolas. The setup is shown below, Fig. 2.13.

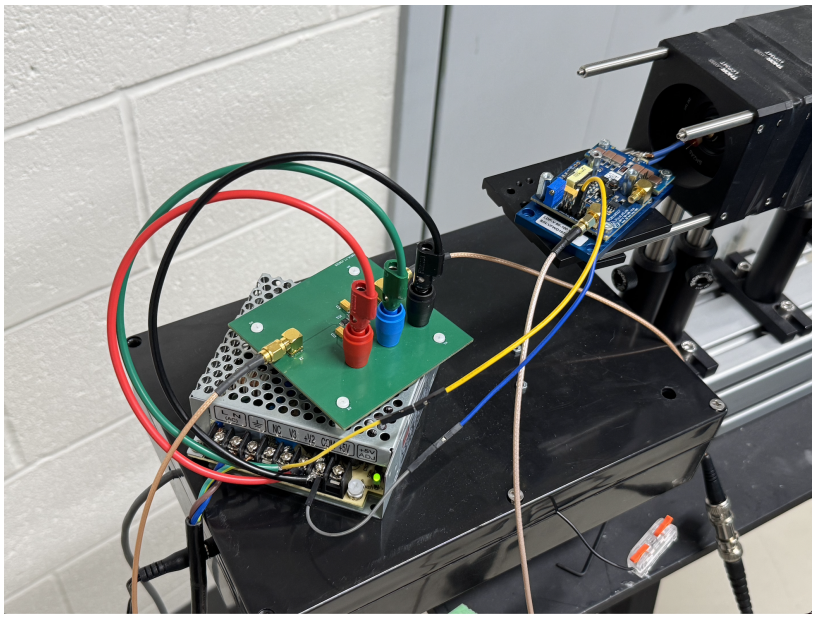
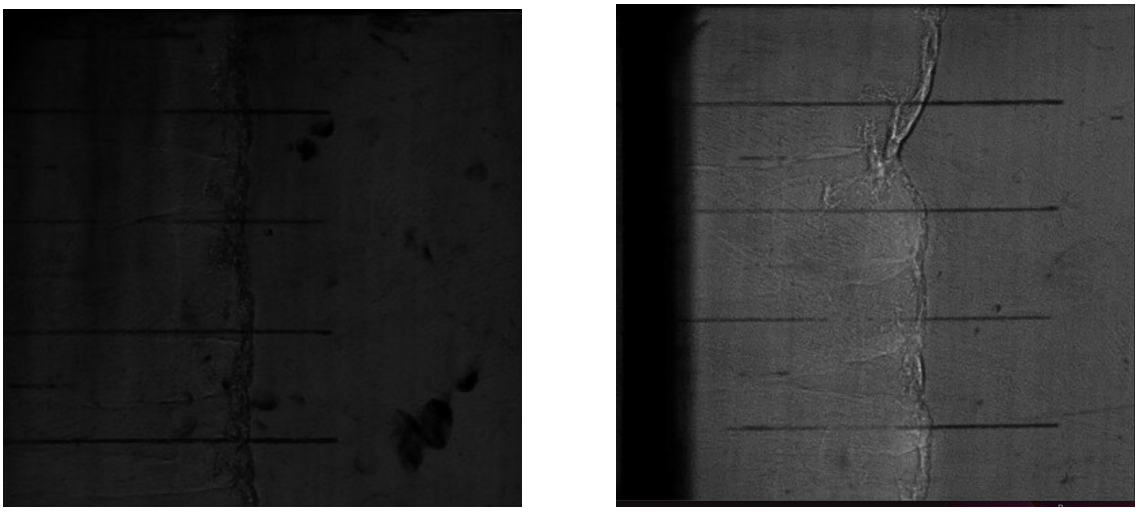


Figure 2.13: The image shows how the PCB, power supply, Picolas, and the light source were connected

The light source was successfully driven with an ON time of 100 nanoseconds and a signal rise time within the accepted range. A detonation test using methane was then conducted with the PCB and LED driver connected to the light source. The camera was set to a frame rate of 100,000. Shown below is a comparison of the results with an without using using the pulsed light source for the same combustible gas and the same frame rate, Fig. 2.14. There is a clear improvement with the pulsed light source. The image is much more clear and the fine details are more apparent.



(a) (b)

Figure 2.14: Fig. a) is the image without a constant light source and Fig. b) is the image with the pulsed light source. The control parameters were the same for both images. Methane gas used for detonation and the camera set to 100,000 frame/second

2.3 Key Safety Considerations

2.3.1 Light Source

The light source is a red LED that is rated up to 500mA at 3V. The LED will damage the eye if looked at directly. To prevent the possibility of eye damage, red light attenuated glasses were used when the light source was on. A circuit was designed utilizing a current limiting resistor to supply a constant 3V signal at 500mA. The circuit board was connected to a switch that could be controlled from outside the testing area.

2.3.2 Picolas

Operating the Picolas poses safety risks due to the high operating voltage and current at the output and the increase in brightness of the LED when the Picolas is connect. The leads and capacitors near the output are connected to up to 100V and must not be touched when the Picolas is on. To mitigate risks the Picolas is controlled from a room outside the testing area using with a LabVIEW program. Detailed instructions are provided on the Picolas manual to properly set it up without coming into contact with high voltage.

2.3.3 Detonation testing

The safety procedure when running detonation test is as follows:

1. **Initiating a detonation:** When igniting the apparatus mixture, everyone must be in the control room, with the door between the control room and the testing room closed. Everyone in the lab must be notified prior to ignition.

2. **Exhaust:** When filling or evacuating the apparatus, the exhaust pump must be turned on using the switch found beside the doorway in the control room. This must be manually confirmed each time by checking the flow indicator. The exhaust fan should be turned on for the entire duration of testing, but should be switched off before the last person leave for the day. Combustible mixture must not enter the vacuum pump. The exhaust line must be diluted well below the flammability limit.

2.4 Economic Analysis

The cost and description of the components used for both the circuit design and the schlieren setup are shown in Table. 2.1 and Table. 2.2 respectively. The majority of the costs were due to the parts needed for Schlieren. Schlieren demands high precision optical components thus the budget and costs were high. Each component was chosen carefully to avoid purchasing unnecessary components.

The costs for the circuit design overall were quite low, but the current feedback amplifier was as significant portion of the cost. To reduce the costs a amplifier could be designed using transistors. However, finding the correct transistor components and determining the appropriate configuration is challenging. Current mirror configurations are required and for current mirrors to work properly the transistors must be identical. [16] Purchasing transistors from online sources like Digikey does not guarantee that the transistors have the exact same properties even if they are the same part. It was decided that purchasing the current feedback amplifier is a better approach as the simplicity out weights the costs.

PCB design costs

Table 2.1: List of components used for PCB

Component (surface mount)	**PN#**	**Cost (each)**
1kohm Feedback Resistor	CR2010-JW-102ELF	$0.26
0.1µf decoupling capacitor	CL05B104KASNNNC	$0.12
49.9kohm gain resistor	CRCW121049K9FKEA	$0.21
2.5pF capacitor	GRM0335C1H2R5BA01	$0.24
Mounting for SMA cable	SMA-J-P-H-RA-TH1	$11.19
Tantalum Capacitor	TAJC685K050RNJ	$1.65
Current Feedback Amplifier	THS3001IDGR	$20.2
Terminating Resistor	TNPW120649R9BEEA	$0.64
100ohm resistor	CRM2512-JW-101ELF	$0.87
SMA cables	CA2812	$18.05
PCB printing costs	N/A	$7.00

Schlieren components

Table 2.2: List of components used for Schlieren

Component	**Description**	**PN#**	**Cost**
Flat Mirror	Turning mirror to bend the light in an L shape.	#46-655	$336
Parabolic Mirror	Mirrors used for Z-type schlieren. (Already in the lab)	#32-277-522	N/A
Photron S20 Camera	High speed camera for visualizing detonation waves (Already in the lab)	N/A	N/A
Circular Cutoff	Iris used to cutoff 50% of light reaching the camera. Sometimes replaced with knife edge.	ID12	$58.31
Aspheric Condensor Lenses (x2)	Lenses used for light source	ACL504U-A	$64.74
Cage Plates (x4)	Holds optical parts in place	LCP34T	$44.54
Iris	Small circular aperture to create a point source	LCP50D	$225.71
Mounting Posts (x8)	Connect to cage plates for alignment	ER6	$9.36
Cage Cover	Covers optical system from external light	C60L24	$32.94
LED Socket (x2)	Socket mount for soldering to LED	ST05S	$5.00
Adapter for LED	Adapters to mount the LED	SM1A6	$22.82
Adapter for LED	Adapter for mounting LED	SM2A6	$29.10
Red LED	Red LED used for the light source	LED635L	$67.71

Chapter 3

Conclusion

Detonation testing requires a highly accurate and sensitive diagnostic system to achieve the best imaging. Through this work a Schlieren optical system and a high speed current amplifying circuit were designed. The Schlieren system design involved creating a point light source, aligning the parabolic and flat mirrors in an L formation to fit within the constraints of the lab, and applying a cutoff at the focal point of the second parabolic mirror. The Schlieren system is ready to be used within the lab. The best results from the high speed circuit design came from implementing the current feedback amplifier on a PCB. The design is functional however it is recommend that more work should be done to develop a more robust system. This includes: designing an in closure for the PCB and Picolas, adding a secondary output on the PCB for easier connection to different Picolas models, designing a system and set of instructions for safe use of the Picolas.

3.1 Future Work

The project is currently in the transition period from design to implementation. The key activities planned are as follows:

1. **Completion of testing:** The immediate focus is completing the testing for the high speed circuit. More detonation test should be conducted with different set frequencies to determine the best setup.

2. **Designing a more robust Schlieren setup** The current Schlieren optical setup works but can be easily placed out of alignment. It is tricky to re align once it has been moved. A system that clearly indicates the correct position of each optical component is required.

3. **Designing a robust setup for the PCB:** Designing a Faraday cage enclosure, a good wiring system, and a set of instructions for use is necessary for safe operation. .

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Appendix A

Statement of Work and Contributions

I worked with my supervisor over the summer to help set up the lab. Most of my work over the summer revolved around writing the LabVIEW and python code needed receiving data from pressure sensors and synchronizing the triggering of the sensors, the ignition, the camera, and the pulse train for the light source. All signals were being sent and received using NI USB-6356 data acquisition device. I also spent time working on helping the other student in my lab with the gas handling system, solid works designs, and other basic lab setup work. Towards the end of the summer I did some research on schlieren by reading parts of the Schlieren and Shadowgraph techniques book to gain some understanding of how schlieren works. I also worked on the circuit design to a point that I was able to discover what the problem was, but I did not do any significant research in how to approach solving it. The schlieren had not been setup. This project is very much an extension of what I started near the end of the summer and not what I was working on for the majority of the summer.

The first semester my work focued on designing Schlieren system, designing the point light source, and designing the circuit. I completed the point light source,

began setting up Schlieren and completed Shadowgraph, and complete an initial two-layer PCB design. Second semester my work included finishing the Schlieren setup, completing the design for the PCB, and testing the final PCB design. I credit Rajan Punna for helping me setup the Schlieren system. I had designed the system myself but I had some assistance in aligning the optics. Rajan also assisted me in running the detonation tests for Schlieren testing.